CLAIMS

1. An apparatus comprising:

a first circuit configured to generate a clock signal in response to (i) a reference signal, (ii) a sequence of spread spectrum ROM codes, and (iii) a command signal; and

a second circuit configured to synchronize said command signal to a feedback signal, wherein said sequence of spread spectrum ROM codes is generated according to a predetermined mathematical formula and optimized in accordance with predetermined criteria.

2. The apparatus according to claim 1, wherein said apparatus comprises a spread spectrum clock generator circuit, wherein said clock signal is spread spectrum modulated.

3. The apparatus according to claim 2, wherein said spread spectrum modulation of said clock signal can be switched on and off in response to said command signal.

4. The apparatus according to claim 2, wherein said circuit is used with a motherboard or CPU.

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5.   The apparatus according to claim 1, wherein said second circuit is further configured to generate one or more control signals in response to (i) said command signal and (ii) said feedback signal.

6.   The apparatus according to claim 5, wherein said second circuit comprises a first latch.

7.   The apparatus according to claim 6, wherein said second circuit further comprises a second latch.

8.   The apparatus according to claim 3, wherein said predetermined criteria are applied to said clock signal during a transition period when spread spectrum modulation is switching on or switching off.

9.   The apparatus according to claim 1, wherein said predetermined criteria includes a predetermined minimum frequency for said clock signal.

10. The apparatus according to claim 7, wherein said predetermined criteria further includes a predetermined maximum frequency for said clock signal.

11. The apparatus according to claim 1, wherein said predetermined mathematical formula is:

$$\begin{bmatrix} X1(N+1) \\ X2(N+1) \\ X3(N+1) \end{bmatrix} = \begin{bmatrix} 0 & -\dfrac{VCO}{FBD(N+1)} & 0 \\ \dfrac{CP(N+1)}{C1} & -\dfrac{1}{C1 \cdot R1} & -\dfrac{1}{C1 \cdot R1} \\ 0 & \dfrac{1}{C2 \cdot R1} & -\dfrac{1}{C2 \cdot R1} \end{bmatrix} \begin{bmatrix} X1(N) \\ X2(N) \\ X3(N) \end{bmatrix} * \Delta t(N) + \begin{bmatrix} U1(N+1) \\ U2(N+1) \\ U3(N+1) \end{bmatrix} * \Delta t(N) + \begin{bmatrix} X1(N) \\ X2(N) \\ X3(N) \end{bmatrix}$$

12. The apparatus according to claim 1, wherein:

said sequence of spread spectrum ROM codes is optimized using a computer program to simulate transient behavior of said apparatus.

13. An apparatus comprising:

means for generating a clock signal in response to (i) a reference signal, (ii) a sequence of spread spectrum ROM codes and (iii) a command signal; and

means for synchronizing said command signal to a feedback signal, wherein said sequence of spread spectrum ROM codes was

generated according to a predetermined mathematical formula and

optimized in accordance with predetermined criteria.

14. A method for controlling a spread spectrum

transition comprising the steps of:

generating a clock signal in response to (i) a reference

signal, (ii) a sequence of spread spectrum ROM codes and (iii) a

command signal; and

synchronizing said command signal to a feedback signal,

wherein said sequence of spread spectrum ROM codes is generated

according to a predetermined mathematical formula and optimized in

accordance with predetermined criteria.

15. The method according to claim 14, wherein the step

of generating said sequence of spread spectrum ROM codes further

comprises the sub-steps of:

(A) selecting a number of ROM codes to be used to

generate a spread spectrum modulation signal; and

(B) generating said number of ROM codes according to

said predetermined mathematical formula.

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Sub A57 16. The method according to claim 15, wherein the step

of optimizing said sequence of spread spectrum ROM codes further

comprises the sub-steps of:

(A) initializing a phase lock loop (PLL) at power supply

5 ramping;

(B) stabilizing said PLL with spread spectrum modulation

turned off;

(C) loading said sequence of spread spectrum ROM codes;

(D) switching on spread spectrum modulation;

(E) recording transient behavior of said clock signal

until PLL is in spread spectrum steady-state;

(F) switching off spread spectrum modulation;

(G) recording transient behavior of said clock signal

until spread spectrum modulation is completely off;

15 (H) comparing recorded transient behavior to

predetermined criteria;

(I) if the recorded transient behavior does not meet

said predetermined criteria, shifting said sequence of spread

spectrum ROM codes, wherein a last ROM code is moved to a first

20 position and remaining ROM codes are shifted one position forward;

(J) if the recorded transient behavior meets said predetermined criteria, finalizing said sequence of spread spectrum ROM codes; and

(K) repeating sub-steps (D) through (J) until said recorded transient response meets said predetermined criteria.

17. The method according to claim 16, wherein said sub-steps are performed by a computer program.

18. The method according to claim 14, wherein said step of generating said clock signal further comprises the sub-step of controlling a feedback divider with said sequence of spread spectrum ROM codes.

19. The method according to claim 14, wherein the step of synchronizing said command signal to said feedback signal further comprises generating one or more control signals in response to (i) said command signal and (ii) said feedback signal.

20. The method according to claim 19, wherein one or more latches are used.